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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/795,939 | 03/08/2004 | Sarath Kotamreddy | 42P19124 | 1335 |

8791 7590 10/04/2005

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| EXAMINER | |
|---|---|
| NGUYEN, HAU H | |
| **ART UNIT** | **PAPER NUMBER** |
| 2676 | |

DATE MAILED: 10/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/795,939 | KOTAMREDDY ET AL. | |
| | Examiner | Art Unit | |
| | Hau H. Nguyen | 2676 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *18 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

### *Response to Arguments*

1. Applicant's arguments filed July 18, 2005 have been fully considered but they are not persuasive. In response to Applicant's arguments that reference Min (U.S. Patent No. 6,184,907) does not teach a queue mechanism divided to include a first functional unit block (FUB) to perform a first set of functions for the queue mechanism and a second FUB to perform a second set of functions for the queue mechanism, the examiner disagrees. In fact, Min teaches the FIFO buffer 140 including a control logic 320 that generates write control signals (a first set of functions) and read control signals (a second set of functions) (col. 5, lines 24-40). Since the claims do not specify what functions the first FUB or the second FUB are performing, they are given the broadest reasonable interpretation, and therefore, rejections are maintained.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 4, 14, 19, and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Min (U.S. Patent No. 6,184,907).

Referring to claims 1, 2, 4, 14, 19, and 30, as shown in Figs. 1 and 2, Min teaches a chipset 100, comprising a graphics accelerator (graphics engine 120) (a first component), a memory controller 150 (a second component), and a queue mechanism (FIFO buffer 140). FIFO buffer 140, as shown in Fig. 2, comprises a first functional unit 310B, and a second functional

unit 310A, coupled to the graphics accelerator and the memory controller. FIFO buffer 140 also includes a control logic 320 to facilitate an interface between the graphics accelerator 120 (first component) and the memory controller 150 (second component) (col. 3, lines 61-63, and col. 5, lines 16-23). As shown in Fig. 2 in combination with Fig. 3A, Min teach the data is input to the first functional unit 310B from the frame buffer 220 and output to the scan interpolator 170 uni-directionally, and the control logic 320 generates strobe signal and packet associated with the strobe (col. 6, lines 65-67, and col. 7, lines 1-15).

### *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3, 5-13, 15-18, 20-29, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Min (U.S. Patent No. 6,184,907) in view of Cavanna et al. (U.S. Patent No. 6,208,703).

Referring to claim 3, 5-13, 15-18, 20-29, and 31, as cited above, Min teaches a queue mechanism comprising a first functional unit and a second functional unit, wherein the first functional unit block comprising a load pointer (write pointer 330, Fig. 2) to generate write address (location in the storage element to store information), and the second functional unit block comprising an unload pointer (read pointer 350, Fig. 2) to generate read address (location in the storage element to read information from) (see col. 5, lines 40-55). Thus, Min teaches all

the limitations of claims 3, 5-13, 15-18, 20-29, and 31, except that the first functional unit operating based on a first clock domain, and the second functional unit operating based on a second clock domain; a logic to compare the load pointer and the unload pointer; the load pointer is clock crossed to the second clock domain; and the unload pointer is clock crossed to the first clock domain.

However, Cavanna et al. teach first-in-first-out synchronizer wherein, as shown in Fig. 1, comprises on the producer side (first FUB), the single stage FIFO synchronizer includes a write input 27, a write clock (WrtCLK) input 28 (first clock domain), a reset (NotWrtRST) input 29 and data (Din[3..0]) input 30. A NotFull output 26 indicates whether the single stage FIFO synchronizer is ready to receive more data from the producer (to determine a command is present). On the consumer side (second FUB), the single stage FIFO synchronizer includes a read input 19, a read clock (RdCLK) input 22 (a second clock domain), a reset (NotRdRST) input 23 and data (Din[3..0]) output 24. A not empty output 18 indicates whether the single stage FIFO synchronizer is ready to transfer more data to the consumer(to determine availability of storage elements). The single stage FIFO synchronizer includes a comparator 14 and 17 (a match logic for comparing read and write pointers), a synchronizer flip-flop 12, a synchronizer flip-flop 16 (clock gating means), a comparator 17, a write pointer flip-flop 11 (a load pointer), a read pointer flip-flop 21 (an unload pointer), connected as shown in Fig. 1 (col. 5, lines 36-55). Cavanna et al. further teach the two signals (write pointer 32 and a read pointer 31) that cross the clock domain each have only one transition per handshake cycle (col. 6, lines 6-9). Data to be stored in the storage elements is directly flopped in the first clock domain within the second FUB

in the consumer FIFO 122 via the synchronizer FIFO 103 as shown in Fig. 4, and col. 7,lines 25-35, and col. 8, lines 13-27.

Since Min teach a control logic controlling a read pointer and a write pointer for accessing the memory, Cavann et al. teach synchronizing between read and write pointers operated in different clock domains as cited above, it would have been obvious to one skilled in the art to utilize the method as taught by Cavanna et al. in combination with the method as taught by Min in order to permit faster operation of the interface (col. 4, lines 57-63).

***Conclusion***

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 571-272-7787. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 571-272-7778.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D. C. 20231

or faxed to:

(703) 872-9306 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (571)-272-2600.

H. Nguyen

09/29/2005

Matthew C. Bella

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600